

Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 7 and 10-22 are pending in the application, with claims 7 and 13 being the independent claims. Claims 1-6 are sought to be canceled without prejudice to or disclaimer of the subject matter therein. Claims 8 and 9 were previously canceled. New claims 19-22 are sought to be added. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 102

The Examiner has maintained the rejection of claims 1-7 and 10-18 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent Application Publication No. 2002/0122280 A1, now U.S. Patent No. 6,765,771, to Kerr *et al.* ("Ker").

Applicants have amended claim 7 to recite an ESD protection circuit having the following features:

one or more first diodes coupled in series between a supply voltage and a terminal pad, each of said one or more first diodes having an n⁺ and a p⁺ diffusion region in an N-well on a first area of P-substrate;

a second diode coupled to a ground, said second diode having an n⁺ and a p⁺ diffusion region on said first area of P-substrate; and

one or more third diodes coupled in series between said terminal pad and said second diode, each of said one or more third diodes having

an n⁺ and a p⁺ diffusion region on a second area of P-substrate separated by a deep N-well from said first area of P-substrate.

Ker does not teach or suggest the combination of the foregoing features of independent claim 7. Applicants respectfully disagree with the Examiner that "Ker shows strings of thyristors and normal diodes and because the thyristors are disposed in deep n-wells with p-type regions and p-n junctions comprising the thyristors, [Ker] anticipates the entire claimed structure." (Office Action, page 2). At a minimum, Ker fails to show an ESD protection circuit including one or more first diodes, each first diode having an n⁺ and a p⁺ diffusion region in an N-well on a first area of P-substrate, as recited in claim 7.

Furthermore, Ker does not show connecting in series first, second, and third diodes, each having the respective structures recited in claim 7. Rather, Ker describes connecting in series a plurality of ESD protection components, each comprised of a lateral silicon controlled rectifier (SCR) and a deep N-well. (Ker at Abstract). Unlike the first, second and third diodes recited in claim 7, the SCR devices described in Ker are four-layer, three-terminal (i.e., anode, cathode and gate) devices. (Ker at col. 4, lines 2-4, col. 5, lines 5-7 and lines 50-52, and col. 6, lines 8-10). Thus, Ker fails to teach or suggest all of the features of independent claim 7, as amended.

Applicants have also amended claim 13 to recite an ESD protection circuit having the following features:

a first diode in a first N-well on a first area of P-substrate, said first diode having a cathode coupled to a supply voltage;

a second diode in a second N-well on said first area of P-substrate, said second diode having a cathode coupled to an anode of said first diode and an anode coupled to a terminal pad;

a third diode on a second area of P-substrate separated by a deep N-well from said first area of P-substrate, said third diode having a cathode coupled to said terminal pad; and

a fourth diode on said first area of P-substrate, said fourth diode having a cathode coupled to an anode of said third diode and an anode coupled to a ground.

For the same reasons described above with respect to independent claim 7, Ker does not teach or suggest the combination of the foregoing features of independent claim 13. At a minimum, Ker fails to teach or describe an ESD protection circuit having a first diode in a first N-well on a first area of P-substrate, the first diode having a cathode coupled to a supply voltage, and a second diode in a second N-well on the first area of P-substrate, the second diode having a cathode coupled to an anode of the first diode and an anode coupled to a terminal pad, as recited in claim 13.

Since Ker fails to teach or suggest the combination of features of independent claims 7 and 13, as amended, Ker fails to anticipate claims 7 and 13. Furthermore, Ker fails to anticipate claims 10-12 and 14-18 for at least the same reasons as independent claims 7 and 13 from which they depend, and further in view of their own features. Claims 1-6 are sought to be canceled, thereby rendering the rejection of claims 1-6 moot. Accordingly, the Examiner's rejection of claims 1-7 and 10-18 under 35 U.S.C. § 102(b) as being anticipated by Ker is traversed and Applicants respectfully request that the rejection be reconsidered and withdrawn.

Additionally, Ker fails to anticipate new claims 19-22 for at least the same reasons as independent claims 7 and 13 from which they depend, and further in view of their own respective features. Accordingly, Applicants respectfully request the entry of new claims 19-22.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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Date: September 29, 2005

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